5. (Amended) The method according to claim 1 wherein said semiconductor unit is attached to said carrier according to a configuration of bump connection.

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9. (Amended) The method according to claim 1 wherein said semiconductor unit is attached to said carrier according to a configuration of lead-on-chip packaging.

10. (Amended) The method according to claim 1 wherein said carrier is a chip carrier, said semiconductor unit includes at least an electrical connection device located on said first surface, and attaching includes a connecting said electrical connection device to said chip carrier.

11. (Amended) A method for reducing the size of at least a semiconductor unit in a process of lead-on-chip packaging wherein said semiconductor unit includes a first surface, a second surface, and at least an electrical connection device located on said first surface, said method comprising the steps of:

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attaching said semiconductor unit to a chip carrier in such a way that said semiconductor unit and said chip carrier are in a configuration of lead-on-chip, with said first surface facing said chip carrier and said second surface exposed; and

etching said semiconductor unit from said second surface until the size of said semiconductor unit meets an expected specification.

12. (Amended) The method according to claim 11 wherein etching includes applying beams of light on said second surface.

14. (Amended) The method according to claim 11 wherein said expected specification means that the thickness of said semiconductor unit measured relative to said first surface is within a specified range.

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15. (Amended) The method according to claim 11 wherein said configuration of lead-on-chip means that part of said first surface is connectible with said chip carrier via adhesive material and said semiconductor unit is electrically connectible with said chip carrier via said electrical connection device.

16. (Amended) The method according to claim 11 wherein attaching includes a step of